Characterization of Phosphorus Deposition onto Silicon (111) 7x7 Nanostructures for Applications in Quantum Computing

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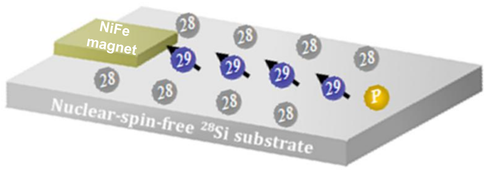
Purpose

All-Silicon Quantum Computer[1]



^{28}Si — ^{28}Si used as a substrate because it is spin-free.

^{29}Si — ^{29}Si used as quantum bits, nuclear spins acting as Boolean logical data.

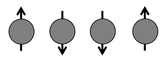
^{31}P — ^{31}P used for initialization, readout, and maintaining an external magnetic field.

NiFe magnet used to generate the external magnetic field of ~7T.

Benefits of an All-Silicon Quantum Computer

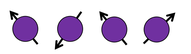
- Quantum superposition allows for parallel processing on a single wire of qubits.
- Techniques for developing silicon already exist.
- Silicon can be scaled to larger devices.

Classical *n*-bit Architecture



Classically, a byte with n bits can represent one of 2^n numbers. Operations must be done one at a time.

Quantum *n*-bit Architecture

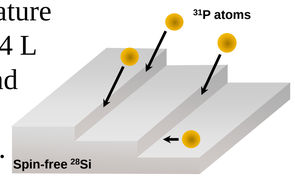


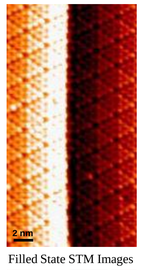
Quantum mechanics allows for one byte to be in a superposition of all 2^n number states. 2^n operations can be done simultaneously.

Experimental Methods

3. Molecular Beam Epitaxy

Slow cooling to room temperature eliminates small defects. 0.014 L doses of ^{31}P are evaporated and adsorbed onto the ^{28}Si step edges at various temperatures.

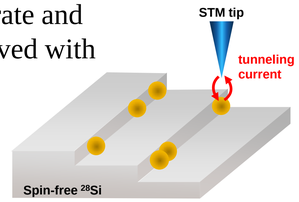


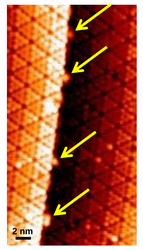


Filled State STM Images

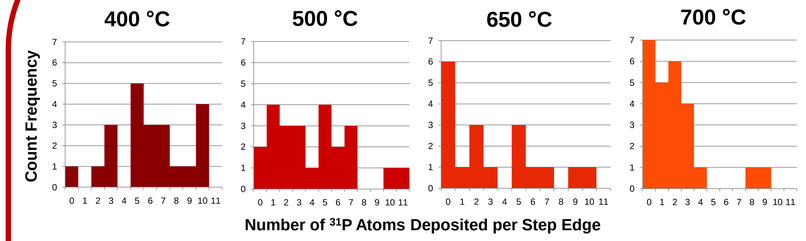
4. Scanning Tunneling Microscopy

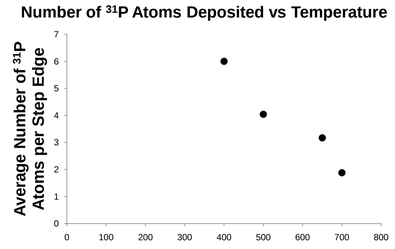
Surface structure of substrate and deposited atoms are observed with the STM. The number of deposited ^{31}P atoms is counted and graphed as a function of temperature.





Results and Conclusions





The deposition rate of ^{31}P does have a temperature dependence in that more ^{31}P atoms are deposited along the ^{28}Si step edges at lower temperatures. At higher temperatures, the ^{31}P atoms have higher thermal energy, which inhibits deposition.

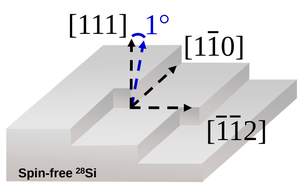
Discussion

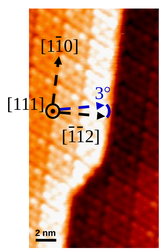
The results for ^{31}P deposition at 400 °C are the most significant, as the ^{29}Si nanowires are grown at this temperature. The willingness of ^{31}P atoms to adsorb onto the ^{28}Si step edges at 400 °C indicates that fabricating the desired ^{29}Si and ^{31}P nanowires is possible and will be a rather straightforward process.

Experimental Methods

1. Mechanical and Chemical Polishing

Ultrafine polishing at a 1° angle in the [111] direction and a 3° tilt in the azimuthal direction produces step edges with kinks.

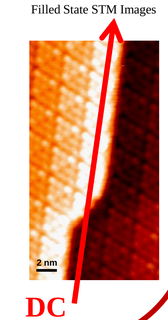




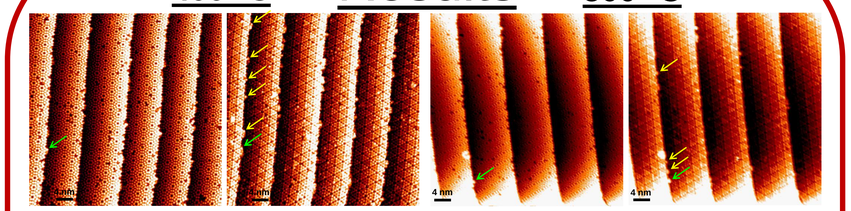
Filled State STM Images

2. Long Duration DC Annealing

Rapid flash heating to 1300°C cleans the substrate. 10 hours of 1.4 A annealing at 800° C in the kink-up direction straightens the edges via electromigration.



Results

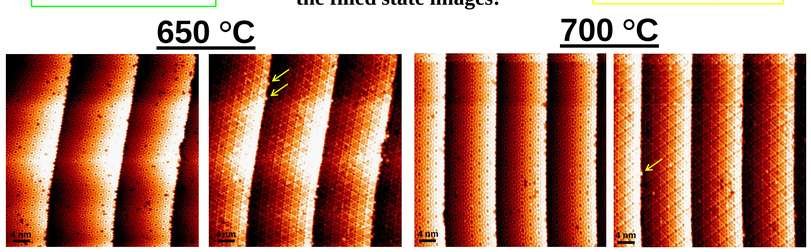


Empty State STM Image | Filled State STM Image | Empty State STM Image | Filled State STM Image

Green arrows indicate atoms that are not ^{31}P.

Phosphorus is visible only in the filled state images!

Yellow arrows indicate atoms that might be ^{31}P.

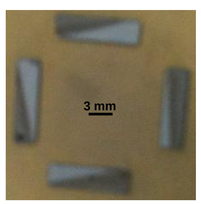


Empty State STM Image | Filled State STM Image | Empty State STM Image | Filled State STM Image

The numbers of ^{31}P atoms per step edge is tallied and displayed in histograms. The results are then averaged and graphed as a function of temperature.

Future Work

- Scanning tunneling spectroscopy of deposited ^{31}P atoms
- Annealing time, deposition time, and azimuthal angle dependence of ^{31}P deposition
- Deposit ^{29}Si nanowires with ^{31}P at the ends



3°, 7°, 11°, 15° azimuthal angle substrates

References

[1] Kohei M. Itoh, Solid State Communications **133**, 747. (2005).

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