Development of Isotopic Spin and Field Effect Transistor Quantum Computers

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Silicon microchips have continued to grow progressively smaller to meet the demands of a competitive market. The next step in development will send the chips from micro-order to nano-order, giving rise to new and challenging complications. Here, two methods are explored to develop such technology. The first involves molecular beam epitaxial (MBE) growth of isotopically controlled Si-based quantum computers. Manual scoring of isotopically pure 28-Si chip followed by kink-up DC correcting and subsequent 29-Si addition leaves equally distributed lines of 29-Si with controllable nuclear spin. Capping the lines on one end with Ni/Fe magnets and on the other end with P atoms, individual spin can be read out and controlled using NMR. The second method involves modifying the traditional Metal Oxide Semiconductor Field Effect Transistor (MOS FET) for successful nano-scale operation. Excessive boron diffusion causes unwanted digital logic stage switching in nano-order MOS FET, so methods to control boron diffusion, transient and oxygen enhanced diffusion, are studied.

Quantum Computers

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Abstract

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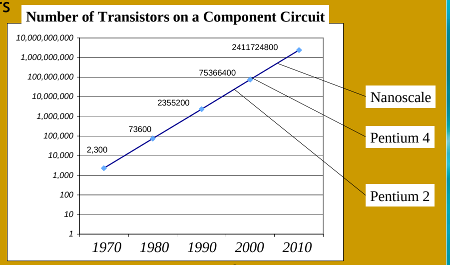
Background

- Gordon Moore's Law: Market transistors need to progressively decrease in size by a factor of two every two years



-Quantum Challenge: Progressing from micro to nanoscale transistors presents new physical and methodological hurdles

-Adaptation versus Innovation: Creating new transistor designs or reinventing old ones

The All-Silicon Model

- 29Si atoms are positioned regularly in chains in a 7-Tesla magnetic field

- A 2-Tesla Ni/Fe magnet at one end of the chain individualizes the spin of each 29SI atom

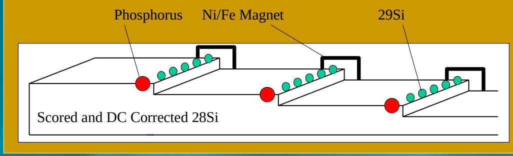
- Nuclear Magnetic Resonance (NMR) is used to locate each 29Si atom and control its spin direction

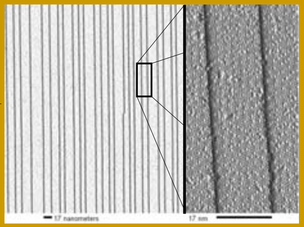
- A phosphorus atom at the opposite end of the chain allows NMR to differentiate between multiple chains

- In the coming years, it is projected that exact positioning of 29Si and precise NMR readout will allow development of the first working All-Silicon Quantum Computer

Building The All-Silicon Model

1. Manual scoring of 28Si chips produces regular step arrays
2. Subsequent DC heating corrects nanoscale imperfections
3. Controlled exposure to natural Silicon allows chains of 29Si to form on the apex of each step

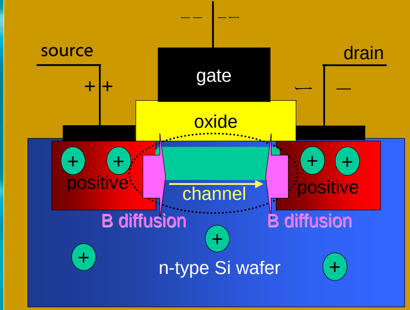




MOS FET Model

(Metal Oxide Semiconductor Field Effect Transistor)

MOS FET functionality:



1. A current source and drain are connected to a silicon wafer

2. Positively charged B atoms are implanted in a neutral Si wafer at the source and drain

3. An oxide layer is added above the channel between the source and drain

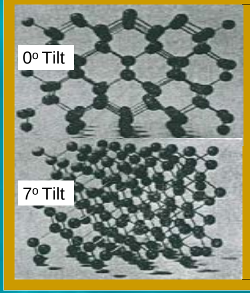
- When voltage is applied to the gate above the oxide layer, positive boron atoms accumulate between the source and drain, allowing the flow of current

- Gate voltage therefore controls the switch between transistor binary states

Nanoscale challenge:

- Annealing purifies transistors, but it also causes B atoms to diffuse
- Nanoscale channels carry current as a result of B diffusion
- The binary state becomes fixed; it is independent of gate voltage
- Boron diffusion must be controlled for nanoscale MOS FET to work

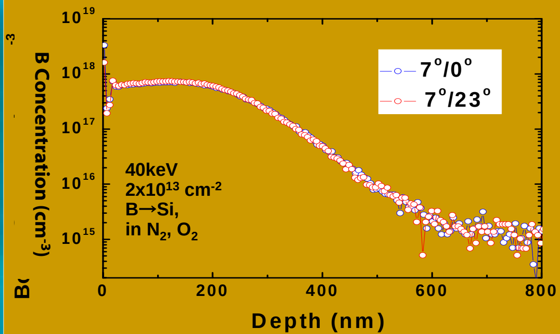
Boron Diffusion



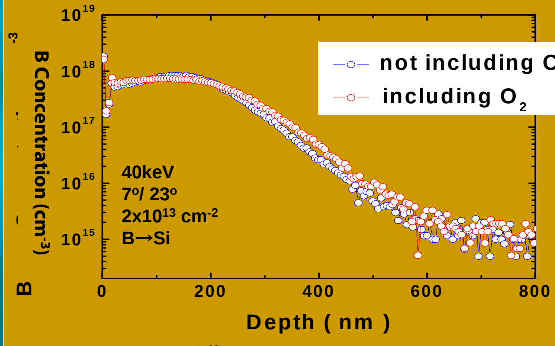
Three branches of diffusion studied

1. **The influence of the B ion implantation damage on TED**
   (Transient Enhanced Diffusion) Tilt 7º/ Rotation 23º or 7º/0º
2. **The influence of OED during initial annealing**
   (Oxygen Enhanced Diffusion) Affect of presence of 0_2
3. **The influence of SiO_2/Si interface during annealing**
   With or without SiO_2(∼20nm) films on the Si surface

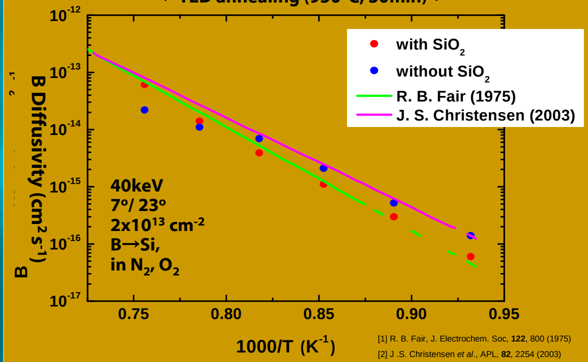
Results



Amount of B ion implantation damage has no correlation with TED



OED increases B ion diffusion



Lack of surface SiO_2 on Si substrate increases B ion diffusion